What is claimed is:

1. A semiconductor integrated circuit comprising a nonvolatile memory enabling electric erase and write over a semiconductor substrate,

wherein said nonvolatile memory comprises a hierarchal bit line structure including first bit lines specific to each of a plurality of memory arrays, a second bit line shared between the plurality of memory arrays, a first selector circuit selecting the first bit line for each of the memory arrays to couple it to the second bit line, and a plurality of sense amps each of which is arranged between an output of corresponding first selector circuit and the second bit line.

2. The semiconductor integrated circuit according to claim 1,

wherein each of said sense amps is a differential sense amp arranged between a pair of memory arrays adjacent to each other, one input of a pair of differential inputs is a read signal from the first bit line in first one of the memory arrays, and the other input is a reference input from the first bit line in second one of the memory arrays.

3. The semiconductor integrated circuit according to claim 1, further comprising a main amp whose input terminal is coupled to said second bit line.

4. The semiconductor integrated circuit according to claim 3,

wherein said main amp is a differential amp whose

differential inputs are coupled to a pair of second bit lines, one input of the pair of differential inputs is a read signal outputted from a first one of the second bit lines, and the other input is a reference input outputted from a second one of the second bit lines.

5. The semiconductor integrated circuit according to claim 1, further comprising one or more third bit lines for write shared between said plurality of memory arrays, the number of said third bit lines corresponding to the number of parallel write bits to the memory array.

6. The semiconductor integrated circuit according to claim 5, further comprising a disconnect circuit capable of coupling or dis-coupling the corresponding first bit line for each of the memory arrays to/from the third bit line, the disconnect circuit controls dis-coupling the first bit line of the memory array to be read in a read operation from the third bit line.

7. The semiconductor integrated circuit according to claim 6, further comprising a second selector circuit selecting the third bit line by the number of external parallel input/output bits of data, and a verify amp sensing verify read data from the third bit line selected by said second selector circuit.

8. The semiconductor integrated circuit according to claim 1,

wherein first power source wires are provided for every plural sense amps along its parallel direction, second power

source wires wider than the first power source wires are provided in positions spaced from the first power source wires, and the first power source wires are coupled to the second power source wires by third power source wires laid in the first bit line direction.

9. The semiconductor integrated circuit according to claim 8, further comprising:

a plurality of third bit lines for write shared between said plurality of memory arrays in such a manner that one of them is provided for every two first bit lines; and

a disconnect circuit capable of selecting coupling or dis-coupling one third bit line to/from any one of the corresponding two first bit lines in each of the memory arrays.

10. The semiconductor integrated circuit according to claim 9,

wherein said third power source wire is arranged every two first bit lines in therebetween.

11. The semiconductor integrated circuit according to claim 6, further comprising:

a first address decoder being used for in a read operation for selecting the word line, the first bit line, the disconnect circuit and the sense amp; and

a second address decoder being used for in a write operation for selecting the word line and the disconnect circuit.

12. The semiconductor integrated circuit according to claim 11,

wherein each of said first address decoder and second address decoders includes address code logic performing address mapping so that the memory arrays, each of which couples to the one sense amp via said first bit lines therein, are arranged not consecutive addresses.

13. The semiconductor integrated circuit according to claim 12,

wherein in a read operation, the first address decoder holds an address decode signal and a select signal of the first bit line for each of the memory arrays corresponding to the change of an address signal during the number of cycles necessary for the read operation, and responds to the change of the address signal to operate said sense amp with delay.

14. The semiconductor integrated circuit according to claim 12,

wherein in a read operation, the first address decoder selects, in parallel, word lines and first bit lines according to an address and the next address, each of which is specified by address signals, drive controls the driving of the second bit line of the respective sense amps corresponding to said specified address and continuously drive controls corresponding to said next address.

15. The semiconductor integrated circuit according to claim 12, further comprising a central processing unit capable of accessing said nonvolatile memory on said semiconductor substrate.

16. The semiconductor integrated circuit according to claim 15,

wherein the memory arrays of part of said plurality of memory arrays are used as a data area, the remaining memory arrays are used as a management area, and said management area is a storage area of a rewrite sequence control program for rewriting the data area,

wherein said central processing unit reads and executes the rewrite sequence control program from said management area and enables rewrite control of the data area.

17. A semiconductor integrated circuit comprising: a nonvolatile memory enabling electric erase and write; and a central processing unit capable of accessing said nonvolatile memory on a semiconductor substrate,

wherein said nonvolatile memory comprises a hierarchal bit line structure including first bit lines specific to each of a plurality of memory arrays, a second bit line shared between the first bit lines of the plurality of memory arrays, and a sense amp arranged between said first bit line and second bit line, and the number of said second bit lines is smaller than the parallel write bit number to the memory array.

18. The semiconductor integrated circuit according to claim 17, further comprising a third bit line for write shared between said plurality of memory arrays.

19. The semiconductor integrated circuit according to claim 18, further comprising a disconnect circuit capable of

connecting and disconnecting the corresponding first bit line for each of the memory arrays to/from the third bit line, the disconnect circuit controls dis-coupling the first bit line of the memory array to be read in a read operation from the third bit line.

20. A semiconductor integrated circuit comprising a nonvolatile memory enabling electric erase and write on a semiconductor substrate,

wherein said nonvolatile memory comprises a hierarchal bit line structure including first bit lines specific to each of a plurality of memory arrays, a second bit line shared between the first bit lines of the plurality of memory arrays, and a sense amp selectively amplifying data read from said first bit line to output the amplified data to the second bit line.

21. A nonvolatile memory device comprising a controller, and one or more nonvolatile memories,

wherein each of said nonvolatile memory is divided into a plurality of memory arrays and includes memory arrays belonging to a first group, and memory arrays of a second group including memory arrays corresponding to the respective memory arrays belonging to said first group,

wherein said controller can control, in parallel, a first access operation to first memory arrays belonging to said first group and a second access operation to third memory arrays except for the first memory arrays and second memory arrays, corresponding to the first memory arrays, belonging to the second

group.

22. The nonvolatile memory device according to claim 21,

wherein a plurality of sense amps are arranged between the memory arrays belonging to said first group and the corresponding memory arrays of the second group,

wherein each of the memory arrays includes a plurality of first bit lines and the first bit lines of the memory arrays of the first group and the first bit lines of the corresponding memory arrays of the second group are coupled to the input terminals of said sense amps,

wherein the outputs of said sense amps are coupled to the second bit lines,

wherein said first and second bit lines are used for a read operation and the third bit line is used for a write operation.

23. A semiconductor integrated circuit comprising a nonvolatile memory enabling electric erase and write on a semiconductor substrate,

wherein said nonvolatile memory comprises a hierarchal bit line structure including first bit lines specific to each of a plurality of memory arrays, a second bit line shared between the plurality of memory arrays, a third bit line shared between the plurality of memory arrays, and a sense amp selectively amplifying data read from said first bit line to output the amplified data to the second bit line in a first read operation and to output the data to the third bit line in a second read operation.

24. The semiconductor integrated circuit according to claim 23,

wherein said first read operation is a read operation for outputting read data to the outside of the semiconductor integrated circuit,

wherein said second read operation is a verify read operation for deciding, based on the read data in data write into the memory array, whether a write operation is continued or not.

25. The semiconductor integrated circuit according to claim 23,

wherein said sense amp includes a selector circuit for amplifying data read from said first bit line to select whether the amplified data is outputted to said second bit line or said third bit line,

wherein said selector circuit selects to output a signal to either the second bit line or the third bit line based on a predetermined select signal.